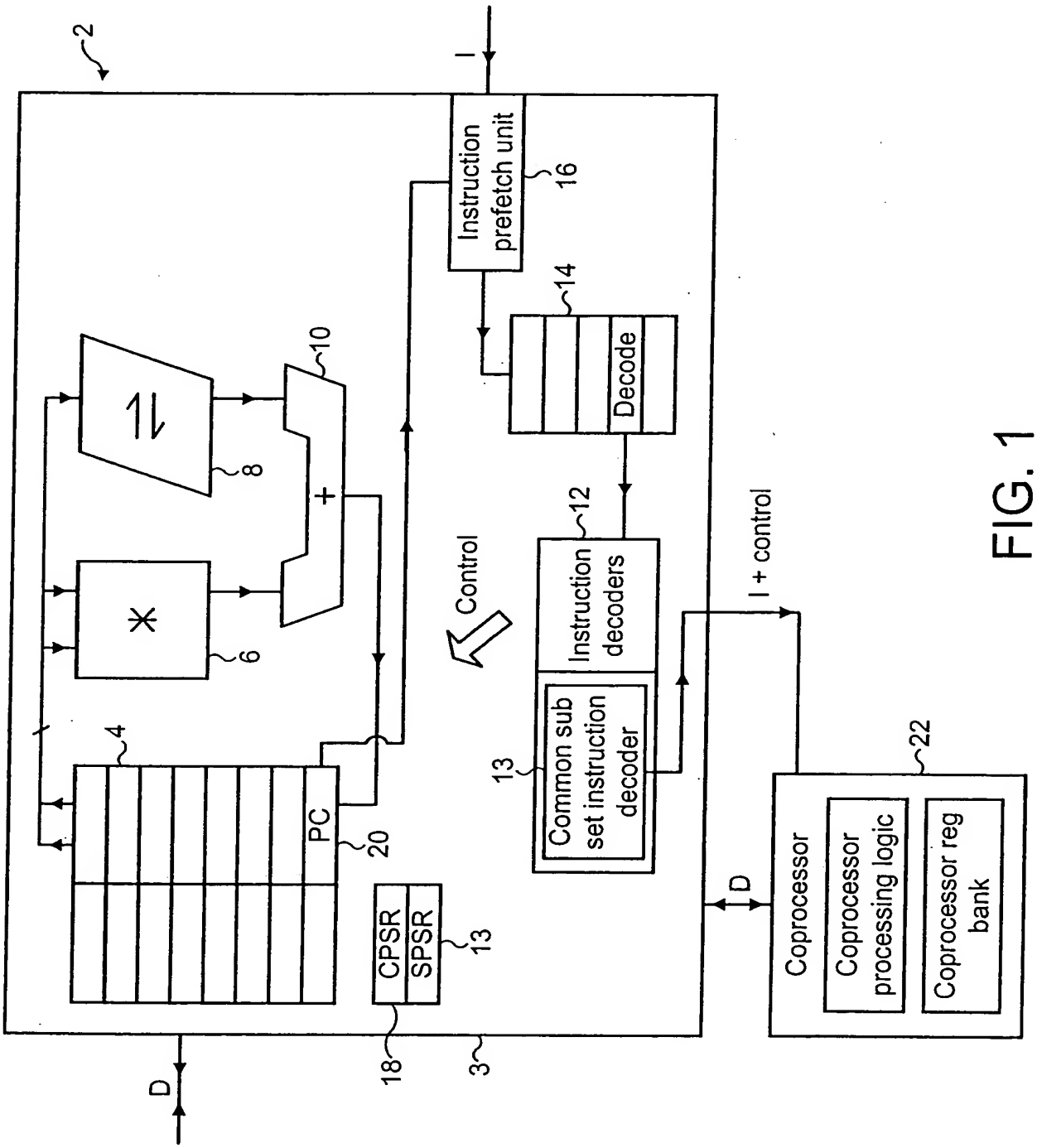
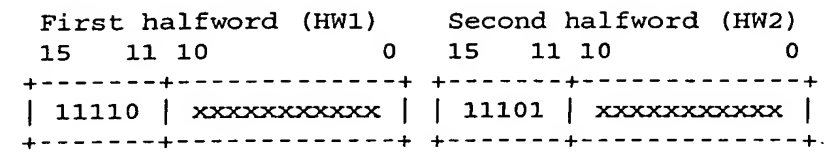

2
I
Instruction prefetch unit
16
14
Decode
10
8
6
4
PC
20
Control
12
Instruction decoders
13
Common sub set instruction decoder
I + control
22
Coprocessor
Coprocessor processing logic
Coprocessor reg bank
D
CPSR
SPSR
13
18
3
D

FIG. 1

BL instruction:




BLX instruction:

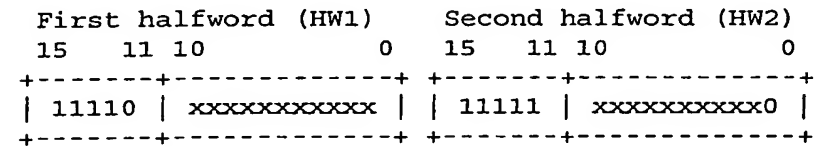
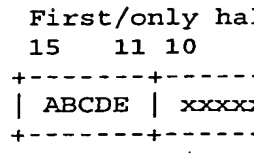



FIG. 2
PRIOR ART

16-bit instruction if ABCDE is in range 00000 to 11100:




32-bit instruction if ABCDE is 11101, 11110 or 11111:

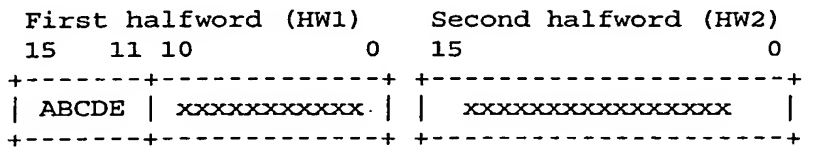
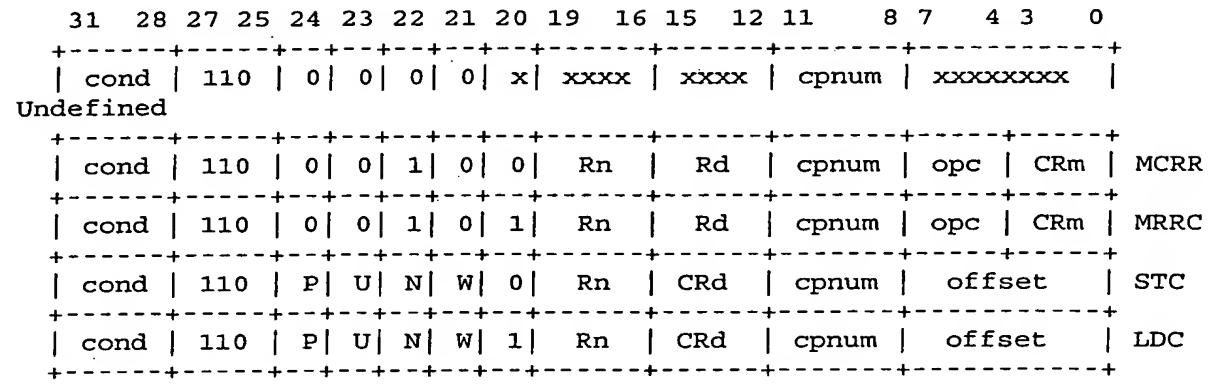



FIG. 3

ARM coprocessor instructions with bits[27:24] = 1100 or 1101:




Note: (P,U,W) != (0,0,0) on the LDC and STC rows.

ARM coprocessor instructions with bits[27:24] = 1110:

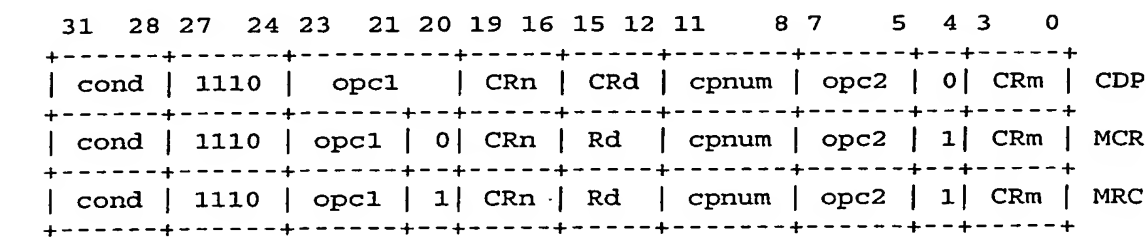



FIG. 4
PRIOR ART

Coprocessor instructions in the enhanced Thumb instruction set:

With HW1[11:8] = 1100 or 1101:

| First halfword (HW1) | | | | | | | | | | | Second halfword (HW2) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 12 | 11 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 0 | 15 | 12 | 11 | 8 | 7 | 4 | 3 | 0 | |
| 111x | 110 | 0 | 0 | 0 | 0 | x | xxxx | | | | xxxx | cpnum | xxxxxxxx | | | | | | Undefined |
| 111x | 110 | 0 | 0 | 1 | 0 | 0 | Rn | | | | Rd | cpnum | opc | | | CRm | | | MCRR |
| 111x | 110 | 0 | 0 | 1 | 0 | 1 | Rn | | | | Rd | cpnum | opc | | | CRm | | | MRRC |
| 111x | 110 | P | U | N | W | 0 | Rn | | | | CRd | cpnum | offset | | | | | | STC |
| 111x | 110 | P | U | N | W | 1 | Rn | | | | CRd | cpnum | offset | | | | | | LDC |

Note: (P,U,W) != (0,0,0) on the LDC and STC rows.

With HW1{11:8] = 1110:

| First halfword (HW1) | | | | | | | | | | Second halfword (HW2) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 15 | 12 | 11 | 8 | 7 | 5 | 4 | 3 | 0 | | 15 | 12 | 11 | 8 | 7 | 5 | 4 | 3 | 0 | |
| 111x | 1110 | opc1 | | | CRn | | | | | CRd | cpnum | opc2 | | | 0 | CRm | | | CDP |
| 111x | 1110 | opc1 | | 0 | CRn | | | | | Rd | cpnum | opc2 | | | 1 | CRm | | | MCR |
| 111x | 1110 | opc1 | | 1 | CRn | | | | | Rd | cpnum | opc2 | | | 1 | CRm | | | MRC |

FIG. 5

| ARM unconditional CDP instruction | | | | | | | | | Byte address | Thumb unconditional CDP instruction | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | 5 | 4 | 3 | 0 | | | | | | 7 | 5 | 4 | 3 | 0 | | | | | |
| opc2 | | 0 | CRm | | | | | | A | opc1 | | CRn | | | | | | ) | |
| CRd | | cpnum | | | | | | | A+1 | 111x1110 | | | | | | | | ) | HW1 |
| opc1 | | CRn | | | | | | | A+2 | opc2 | | 0 | CRm | | | | | ) | |
| 111x1110 | | | | | | | | | A+3 | CRd | | cpnum | | | | | | ) | HW2 |

FIG. 6

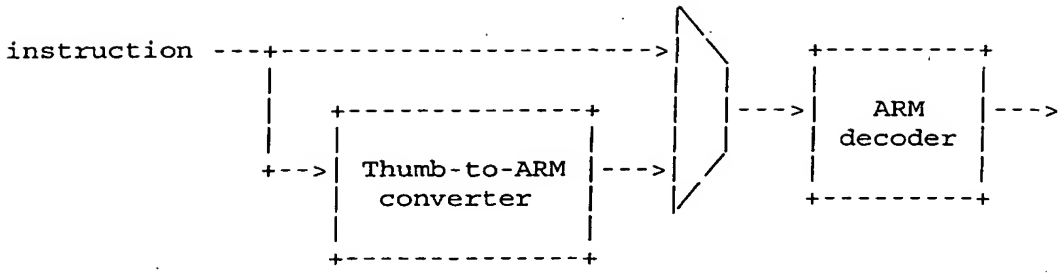



FIG. 7
PRIOR ART

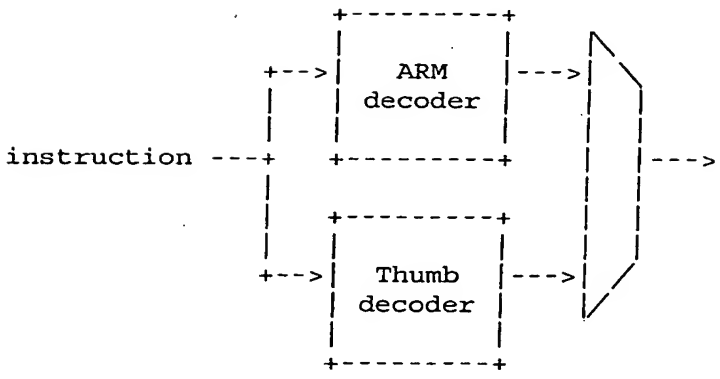



FIG. 8
PRIOR ART

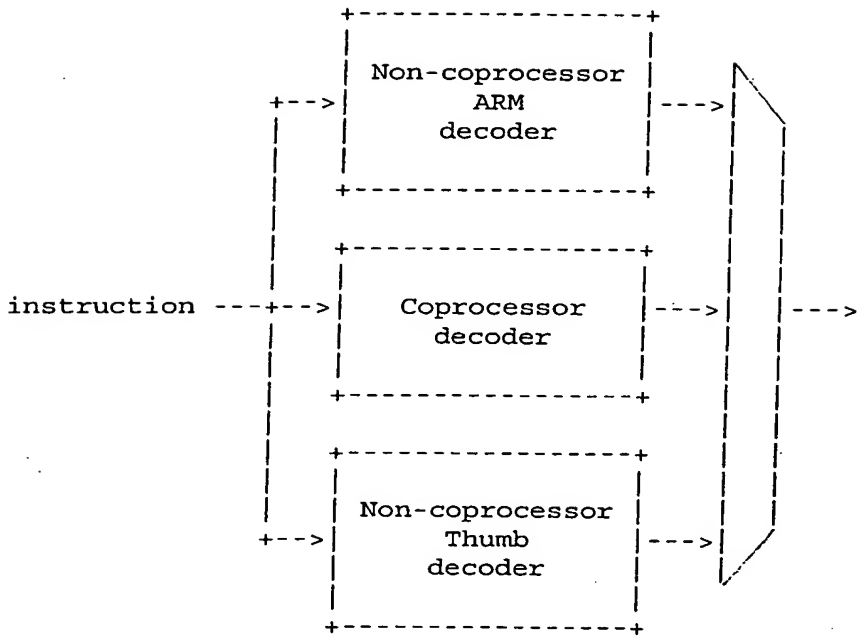

Non-coprocessor
ARM
decoder
instruction
Coprocessor
decoder
Non-coprocessor
Thumb
decoder

FIG. 9

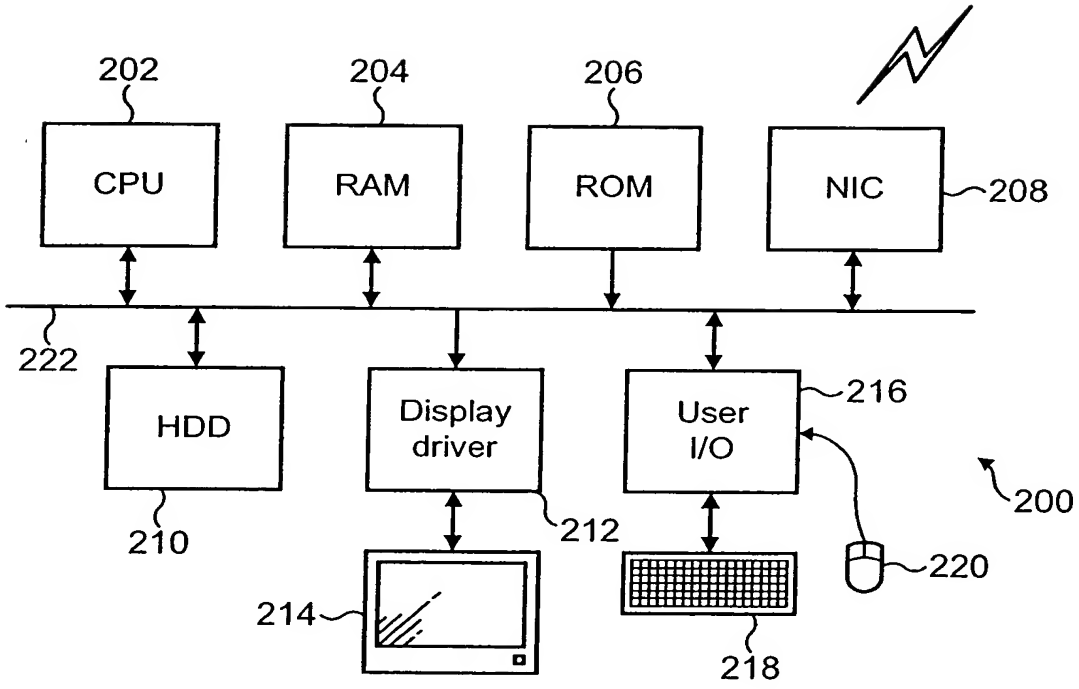

202
204
206
CPU
RAM
ROM
NIC
208
222
HDD
Display driver
User I/O
216
200
210
212
214
220
218

FIG. 10